Excellent Phosphorus Doped LPCVD Polysilicon Passivated Contacts via Low Pressure Oxidation

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***Abstract* — This work presents the investigation of low pressure in-situ thermal oxidation as the interfacial oxide for n+ polysilicon-oxide passivated contact structure, achieving excellent surface passivation below 1 fA·cm^{-2} and contact resistivity below 1 mΩ·cm^2. The results from the process optimisation are presented in detail, showing the importance of accurate control of oxidation conditions, and presenting the correlation to the electrical properties. Additionally, a method of fabricating contact resistivity structures from symmetrical photoconductance decay lifetime samples, and the extraction of the specific contact resistivity using 3D numerical simulation is presented.**

I. Introduction

Application of passivated contacts to solar cells requires fulfilment of two key electrical requirements; having sufficiently low surface recombination and low contact resistivity. In the case of a full area rear contact cell, the surface passivation is the key property, and a high contact resistivity below 100 mΩ·cm^2 is generally tolerable. However, Poly-Ox contacts are increasingly being explored for application under metal fingers to form local contacts such as in interdigitated back-contact (IBC) and bifacial passivated emitter and rear cell (PERC) solar cells. The small contact area necessitates lower contact resistivity in order to avoid high series resistance losses. However, investigation of polysilicon contacts, and other forms of passivated contacts in literature suggests that some trade-off between surface passivation and contact resistivity is inevitable, requiring careful optimisation for application to specific cell designs [1-5].

A significant advancement in passivated contact technology is presented, where very low surface recombination, and very low contact resistivity is achieved. The novelty of this work lies in the use of low-pressure (< 600 mTorr) thermal oxidation to control the growth conditions for the interfacial oxide grown at temperatures between 700 - 850 ^{o}C. Furthermore, as it is performed in-situ to the polysilicon deposition the oxide is not exposed to the atmosphere prior to be capped with polysilicon, allowing fine control of ultra-thin (<1 nm) high quality oxide layer. The experimental details and excellent electrical properties of the film achieved with this technique is presented, along with discussions on the measurement methods, and observed correlation between electrical characteristics to the process conditions.

II. Surface Passivation

Starting with 1 Ω·cm and 100 Ω·cm n-type wafers, we grow the interfacial oxide under low pressure condition within the LPCVD furnace, where the oxidation temperature is varied, while the oxidation time and pressure are held at 10 minutes, and 600 mTorr respectively. Polysilicon is then deposited at 520 ^{o}C in-situ to the oxidation process without breaking vacuum. Phosphorus diffusion is carried out in a standard diffusion furnace using liquid $POCl_3$ source. The deposition temperature is done at a range of temperatures, and samples are subsequently annealed at 900 ^{o}C. J_0 measurements are done using transient-mode photoconductance-decay method, and extracted at an excess carrier density, Δn of 3x10^{15} cm^3. The presented sheet resistivity, R_{sheet} is deduced from the PCD measurement after subtracting the wafer bulk resistivity and divided by two to represent the polysilicon stack of a single side.

To investigate both the surface passivation and the contact resistance of the sample, we vary the oxidation temperature and phosphorus diffusion temperature. By doing so, we control two key parameters of doped poly-ox stack: the oxide thickness; and the doping profile. Figure 1(a) and (b) presents the results of this experiment, where J_0 and R_{sheet} are plotted against the oxidation and phosphorus diffusion temperatures performed on 1 Ω·cm and 100 Ω·cm n-type wafers.

The samples of both resistivity exhibit a strong correlation to both oxidation and diffusion temperatures. It appears that the condition for excellent surface passivation (eg: where J_0 is below 5 fA·cm^{-2}) is rather robust and can be achieved over a broad range of oxide temperatures (and therefore thickness) and phosphorus diffusion temperatures. A strong correlation is also observed between J_0 and R_{sheet}, where samples with good J_0 typically also have high R_{sheet}. The lowest J_0 was measured to be 0.3 ± 0.8 fA·cm^{-2} with an R_{sheet} of 423 Ω/□ on the sample

with 750 °C in-situ oxidation and 750 °C phosphorus diffusion. The observed correlation to high R_{sheet} is consistent with other investigations in literature which points out the role of the interfacial oxide as a dopant diffusion barrier [1] so as to limit the amount of phosphorus dopants penetrating into the silicon bulk, causing an increase in Auger recombination within the diffused region of the bulk wafer. A low R_{sheet} therefore suggests that the interfacial oxide is too thin, allowing significant diffusion into the base wafer material.

A more in-depth investigation and discussions on the correlation between the R_{sheet} and J_0 to the doping profile as measured via ECV is presented in another publication by the authors [6].

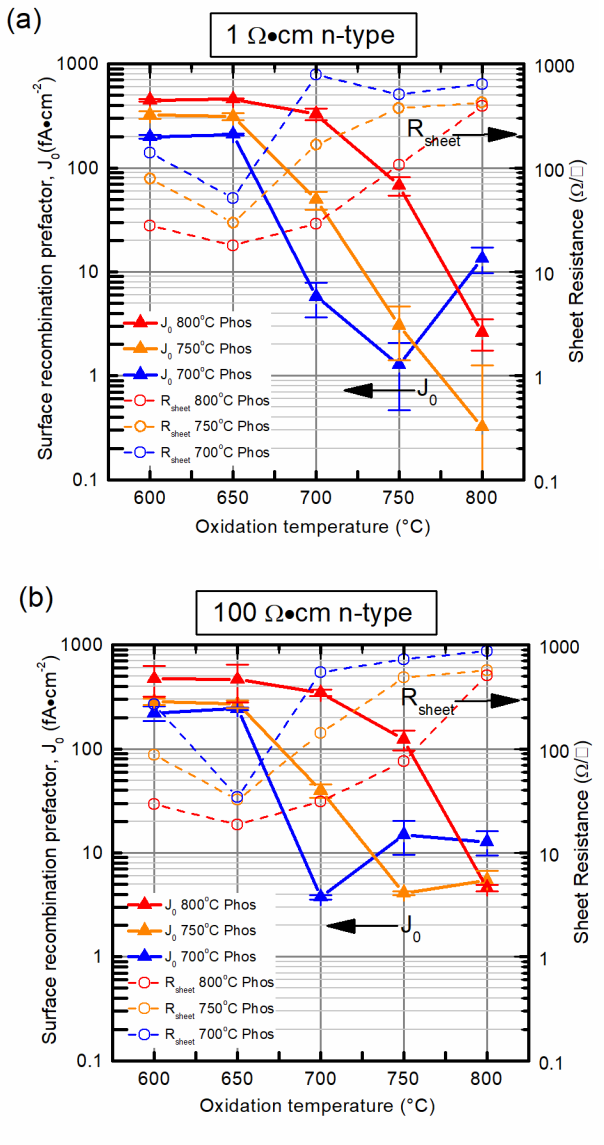

Figure 1: J_0 and R_{sheet} versus oxidation temperature for a range of phosphorus diffusion temperature on (a) 1 Ω·cm and (b) 100 Ω·cm n-type wafer.

III. Contact Resistance Method & Results

In order to obtain an accurate representation of the electrical properties of the film, J_0 and specific contact resistivity, ρ_c were both measured from the same sample. This is achieved here by fabricating contact resistance measurement structures as presented by Cox and Stracks (C&S) [7] on the 1 Ω·cm lifetime samples by directly evaporating Al over the front surface through a shadow mask, and over the entire rear surface, as illustrated in Figure 2(a). It is important to note that extraction of ρ_c directly from this structure is difficult as one would have to account for the spreading resistance within the front polysilicon layer, the base Si wafer, and the carrier transport across the thin tunnel oxide with a possibly non-linear resistance characteristic (non ohmic).

To simplify the problem, several microns of the front surface was etched using a modified TMAH solution[8] while leaving the Al intact. An illustration of the cross section of the sample after etching is presented in Figure 2(b).

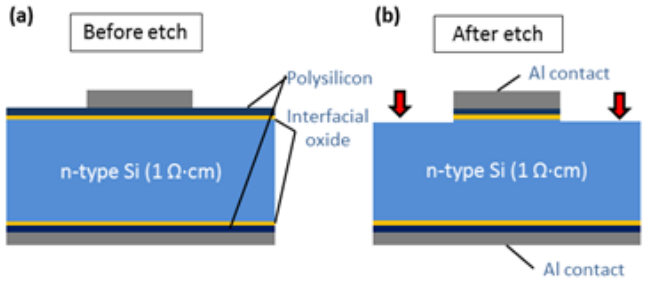

Figure 2: Structure for contact resistivity measurement, (a) before and (b) after modified TMAH etch to stop lateral carrier transport.

The use of varied dot sizes allows deduction of the contact resistance from the spreading resistance within the silicon wafer. However, although the original analytical model as presented in [7] can provide a seemingly good fit, it must be noted that it assumes a non-negligible rear contact resistance, such as for the samples in this work. Figure 3 illustrates the discussed errors when applying in the standard C&S method to a front-rear symmetrically contacted sample. Firstly, it demonstrates the significant difference in measured resistance before and after etching. Secondly, we demonstrate here that a good fit (to the etched sample) is possible but can leads to significant overestimate of ρ_c for certain conditions.

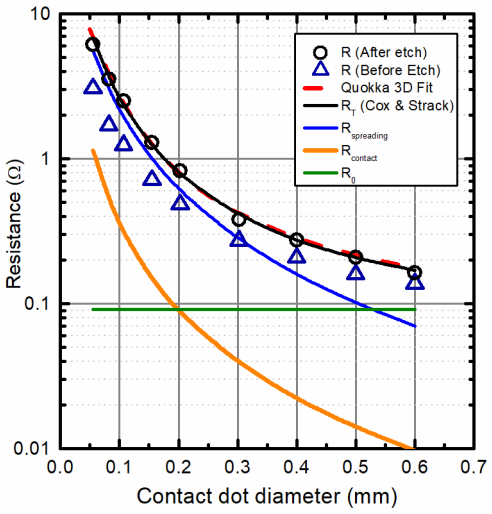

Figure 3: Comparison of measured resistance before and after TMAH etching to remove polysilicon surrounding contact dots.

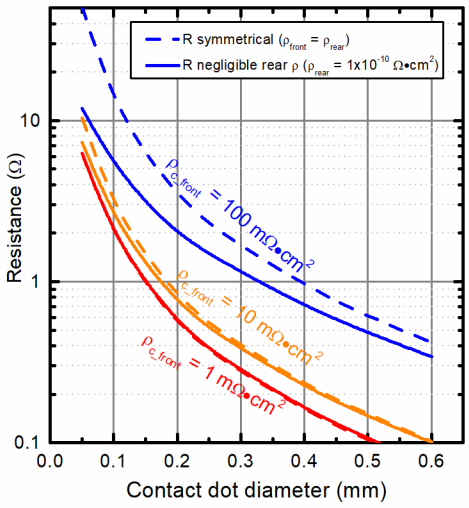

Figure 4: 3D simulation of C&S dot structure measurements comparing the standard structure of having negligible rear contact resistance to a front-rear symmetrical contact structure.

To examine this systematic error, we utilize 3D numerical simulation in Quokka [9] to generate the relationship between measured resistance versus the front contact dot size for two conditions: Symmetrical ρ_c, where $\rho_{c,front} = \rho_{c,rear}$; and negligible rear contact $\rho_{c,rear}$ of $1x10^{-10}$ Ω·cm^2. The simulation results are presented in Figure 4 for three different $\rho_{c,front}$. There are two main observation to be made: Firstly, as expected, a significant difference in the measured resistance is expected when the ρ_c is large, Secondly, the simulation suggests that there is negligible differences when ρ_c = 1 mΩ·cm^2. This is rather expected as well since the contribution of the large rear contact area becomes negligible even in the symmetrical contact structure, and the resistance in the system is now dominated by the spreading resistance within the base Si wafer. We can conclude from such simulation that at higher ρ_c, a non negligible rear contact resistance contributes significantly to the resistive loss, translating to significant errors when fitted to the unmodified Cox and Stracks model. The difference is small when ρ_c is also small, but the overall error is large as the C&S method typically does not provide good accuracy below 1 mΩ·cm^2 as the resistance in the bulk dominates.

Therefore, to avoid unnecessary systemic error, the most accurate method is to deduce ρ_c is to fit the measured experimental results with 3D simulation, performed here using Quokka [10]. Within the simulation, the geometrical structures are reproduced using measured values the input parameters such as the wafer resistivity, wafer thickness, base resistance and metal contact dot sizes. The simulation assumes identical front and rear ρ_c, which is varied iteratively until a good fit is obtained to the experimental data.

The deduced ρ_c from the 1 Ω·cm lifetime samples of Figure 1 is presented in Figure 5, which shows excellent ρ_c < 1 mΩ·cm^2 is measured for a large range of samples.

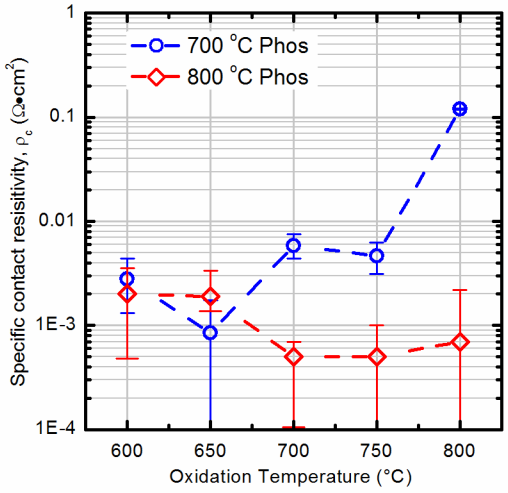

Figure 5: Deduced ρ_c from fitting to 3D simulation.

IV. Summary

A summary of data where both ρ_c and J_0 are measured on the same sample is presented in Figure 6, noting that excellent surface passivation below 3 fA·cm^{-2} and low contact resistivity below 1 mΩ·cm^2 is achieved simultaneously, representing among the lowest values measured in combination.

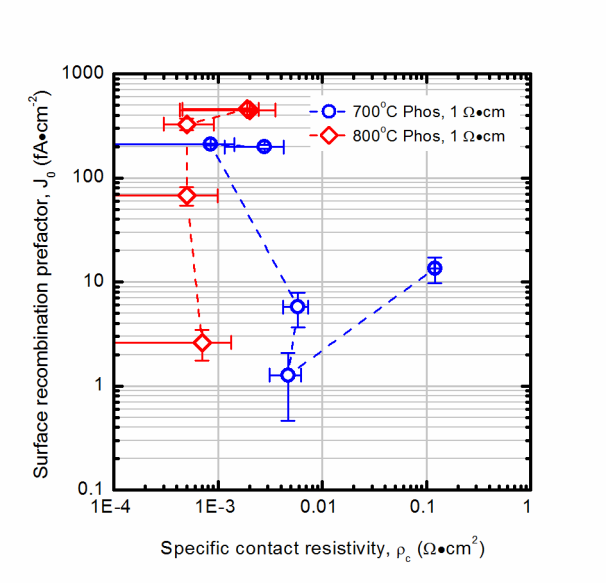

Figure 6: Summary of J_0 and ρ_c measured in this work.

We have also presented an extensive investigation into the use of the Cox and Strack analytical model for a front-rear symmetrically contacted structure, which concludes that significant error is likely for moderate to large ρ_c, and an accurate measurement is possible only when ρ_c is very small (eg: ρ_c ~ 1 mΩ·cm^2). Therefore, the best option is to deduce ρ_c for non-standard structures is to utilize 3D ohmic simulation, which have now become staple analysis tools available to most researchers and institutes.

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